Amendment to Claims

1 (previously presented). A method for fabricating an integrated circuit comprising a nonvolatile memory comprising a nonvolatile memory cell comprising two floating gates, a select gate, and two control gates, the nonvolatile memory further comprising a first peripheral transistor, the method comprising:

(a) forming a dielectric layer on a semiconductor substrate, the dielectric layer comprising a first dielectric region ("select gate dielectric") and a second dielectric region ("first peripheral transistor gate dielectric"), wherein the select gate dielectric and the first peripheral transistor gate dielectric are formed simultaneously;

(b) forming a first layer over the dielectric layer and patterning the first layer to provide (i) the select gate on the select gate dielectric, and (ii) a gate for the first peripheral transistor on the first peripheral transistor gate dielectric;

(c) after forming the first layer, forming one or more second layers which provide the floating gates and the control gates for the memory cell, the floating and control gates being provided entirely by the one or more second layers, the floating and control gates comprising no portion of the first layer.

2 (currently amended). The method of Claim 1 wherein the memory cell comprises a continuous channel region of a first conductivity type in the semiconductor substrate, the select gate controls a conductivity of a portion of the channel region, and each of the floating gates overlies a respective other portion of the channel region.

3 (original). The method of Claim 2 wherein the control gates overlie the respective floating gates.

4 (previously presented). The method of Claim 1 wherein the one or more second layers are a plurality of layers.

5 (original). The method of Claim 1 wherein the select gate dielectric and the first peripheral transistor gate dielectric are formed by oxidation of the semiconductor substrate.

6 (original). The method of Claim 5 wherein the select gate dielectric and the first peripheral transistor gate dielectric comprise silicon oxide.

7 (previously presented). The method of Claim 1 further comprising, after forming the first layer, forming a dielectric ("floating gate dielectric") on the semiconductor substrate to separate the floating gates from the substrate, wherein the floating gate dielectric is formed of the same material as the select gate dielectric but is thinner than the select gate dielectric.

8 (original). The method of Claim 1 further comprising forming a second peripheral transistor gate dielectric on the semiconductor substrate for a second peripheral transistor, and forming a gate of the second peripheral transistor on the second peripheral transistor gate dielectric, wherein the second peripheral transistor gate dielectric is made from the same material as the select gate dielectric and the first peripheral transistor gate dielectric but the thickness of the second peripheral transistor gate dielectric is different from the thickness of the first peripheral transistor gate dielectric.

9 (original). The method of Claim 8 wherein the second peripheral transistor gate dielectric is thinner than the first peripheral transistor gate dielectric.

10 (original). The method of Claim 8 wherein the select gate dielectric as at least as thick as a gate dielectric of any peripheral transistor in said memory.

11 (original). The method of Claim 8 wherein the second peripheral transistor gate dielectric is formed after the start of the operation (a).

12 (original). The method of Claim 8 wherein the second peripheral transistor gate dielectric is formed before the operation (b).

13 (original). The method of Claim 8 wherein the gate of the second peripheral transistor is formed by patterning the first layer in the operation (b).

14 (original). The method of Claim 1 wherein the memory cell is one of a plurality of nonvolatile memory cells of said memory, each memory cell comprising two floating gates, a select gate, and two control gates, wherein:

the operation (a) simultaneously forms select gate dielectric for each of the memory cells; and

the operation (b) simultaneously forms the select gate for each of the memory cells on the corresponding select gate dielectric.

15 (original). The method of Claim 1 wherein during a memory cell writing operation, the first peripheral transistor is exposed to a voltage of a higher magnitude than any voltage provided to the memory cell in a reading operation.

16 (original). The method of Claim 15 wherein during the memory cell writing operation, the first peripheral transistor is exposed to a voltage of a higher magnitude than any power supply voltage provided to the nonvolatile memory.

17 (original). The method of Claim 1 wherein the memory is to support a writing operation in which the memory cell is written by a transfer of a charge between one of the floating gates and a channel region of the memory cell, the channel region being located in the semiconductor substrate.

18-29 (canceled).

30 (previously presented). The method of Claim 1 wherein the operation (c) further comprises patterning the one or more second layers to provide the floating and control gates.

31 (previously presented). The method of Claim 1 wherein the first layer patterning comprises:

(b1) patterning the first layer to provide the select gate; and

(b2) patterning the first layer to provide the gate for the first peripheral transistor;

wherein the operation (c) is performed after the operation (b1) but before the operation (b2).

32 (previously presented). The method of Claim 1 further comprising, after forming the first layer but before forming the one or more second layers, forming a dielectric ("floating gate dielectric") on the semiconductor substrate to separate the floating gates from the substrate.

33 (previously presented). The method of Claim 32 wherein the first layer patterning comprises:

(b1) patterning the first layer to provide the select gate; and

(b2) patterning the first layer to provide the gate for the first peripheral transistor;

wherein the floating gate dielectric is formed after the operation (b1).

34 (currently amended). The method of Claim 1 wherein the memory cell comprises a continuous channel region of a first conductivity type in the semiconductor substrate, and each of the floating gates controls a conductivity of a respective portion of the channel region.

35 (previously presented). The method of Claim 34 wherein the select gate controls the conductivity of a portion of the channel region.

36 (previously presented). The method of Claim 35 wherein the channel's portion whose conductivity is controlled by the select gate is between the channel's portions whose conductivities are controlled by the floating gates.

37 (currently amended). The method of Claim 1 wherein the memory cell comprises two source/drain regions and a continuous channel region bordering on the source/drain regions, wherein the channel region has an opposite conductivity type from the source/drain regions, and each floating gate of the memory cell overlies a portion of the channel region.

38 (previously presented). The method of Claim 1 wherein the floating gates are adjacent to respective two opposite sidewalls of the select gate and are insulated from the select gate.